IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Original): A system for generating a histogram of a plurality of power data values, the system comprising:

a processing apparatus receiving the plurality of power data values and converting the plurality of power data values to a plurality of floating-point numbers; and

a memory including a plurality of histogram bins connected electronically to the processing apparatus, wherein the processing apparatus stores counts of the plurality of floating-point numbers using each floating-point number as an address for a corresponding histogram bin in the memory.

Claim 2 (Currently amended): The system of claim 1, wherein the plurality of power data values comprise a plurality of $(I^2 + Q^2)$ data values, wherein each $(I^2 + Q^2)$ data value represents a power value of a signal.

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Claim 3 (Original): The system of claim 2, wherein an exponent and a mantissa in the plurality of floating-point numbers are computed according to the equations:

exponent = 2^E-1 – (number of leading zeros in MS, up to 2^E–1)
mantissa = MS[(N-2^E-1+exp):(N-2^E+exp-M)] for exp>0; or
mantissa = MS[(N-2^E):(N-2^E+1-M)] for exp=0

where E is the number of bits assigned to the exponent, M is the number of bits assigned to the mantissa, MS is a respective ($I^2 + Q^2$) data value in the plurality of ($I^2 + Q^2$) data values, and N is the number of bits assigned to the plurality of ($I^2 + Q^2$) data values.

Claim 4 (Original): The system of claim 3, wherein the total number of histogram bins in the memory is determined by the equation $2^{(E+M)}$.

Claim 5 (Original): The system of claim 3, wherein a maximum bin width for the histogram bins is determined by the equation $10^* \log_{10} (1+2^{-M})$.

Claim 6 (Original): The system of claim 3, wherein a range of histogram bins is determined by the equation $(20 - 10^*2^E)^*\log_{10}(2)$.

Claim 7 (Original): The system of claim 1, wherein a maximum count for the histogram bins is determined by the equation (2^w-1), where w represents a bit width of the memory.

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Claim 8 (Original): The system of claim 2, wherein the processing apparatus comprises:

a field programmable gate array receiving the plurality of $(I^2 + Q^2)$ data values; and

a microprocessor connected electronically to the field programmable gate array, wherein the field programmable gate array and the microprocessor work cooperatively to convert each $(I^2 + Q^2)$ data value to a floating-point number and store counts of the plurality of floating-point numbers using each floating-point number as an address for a corresponding histogram bin in the memory.

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Claim 9 (Currently amended): The system of claim 1, wherein the processing apparatus comprises:

an analog to digital converter receiving an analog immediate frequency signal and converting to a digital immediate frequency signal;

an application specific integrated circuit receiving the digital immediate frequency signal, down-converting the immediate frequency signal to a baseband signal including a plurality of I and Q data values, and calculating the plurality of power data values comprised of a plurality of $(I^2 + Q^2)$ data values<u>, wherein each $(I^2 + Q^2)$ data value represents a power value of the signal</u>;

a field programmable gate array receiving the plurality of $(I^2 + Q^2)$ data values; and

a microprocessor connected electronically to the field programmable gate array, wherein the field programmable gate array and the microprocessor work cooperatively to convert each $(I^2 + Q^2)$ data value to a floating-point number and store counts of the plurality of floating-point numbers using each floating-point number as an address for a corresponding histogram bin in the memory.

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Claim 10 (Currently amended): The system of claim 1, wherein the processing apparatus comprises:

an analog to digital converter receiving an analog immediate frequency signal and converting to a digital immediate frequency signal; and

an application specific integrated circuit receiving the digital immediate frequency signal, down-converting the immediate frequency signal to a baseband signal including a plurality of I and Q data values, calculating the plurality of power data values comprised of a plurality of ($I^2 + Q^2$) data values, converting each ($I^2 + Q^2$) data value to a floating-point number, and storing counts of the plurality of floating-point numbers using each floating-point number as an address for a corresponding histogram bin in the memory, wherein each ($I^2 + Q^2$) data value represents a power value of the signal.

Claim 11 (Original): The system of claim 2, wherein the processing apparatus comprises:

an analog to digital converter receiving a plurality of analog power data values and converting to a plurality of digital power data values comprised of ($I^2 + Q^2$) data values; and

an application specific integrated circuit converting each ($I^2 + Q^2$) data value to a floating-point number and storing counts of the plurality of floating-point numbers using each floating-point number as an address for a corresponding histogram bin in the memory.

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Claim 12 (Currently amended): A method for deriving a power complementary cumulative distribution function (CCDF) from a plurality of power data values, comprising:

a) receiving a power data value;

b) converting the power data value to a floating-point number;

c) reading a location in a memory using the floating-point number as an address for the location in memory;

d) incrementing by one a count read from the location in memory;

e) writing the incremented count to the location in memory; and

f) repeating a through e until all of the power data values in the plurality of power data values have been received, converted, and accumulated in corresponding locations in memory; and

g) generating a histogram of the plurality of floating-point numbers using the memory locations as histogram bins.

Claim 13 (Original): The method of claim 12, further comprising calculating a complementary cumulative distribution function curve from the histogram.

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Claim 14 (Original): The method of claim 13, wherein calculating a complementary cumulative distribution function curve from the histogram comprises calculating an average power for the plurality of power data values according to the equation average power = $\sum (P_i * C_i) / \sum (C_i)$, for i = 1 to K, and K = number of bins, P_i is the power for the ith bin, and C_i is the count for the ith bin.

Claim 15 (Original): The method of claim 14, wherein calculating a complementary cumulative distribution function curve from the histogram comprises grouping the counts in the histogram bins into a plurality of CCDF bins.

Claim 16 (Original): The method of claim 15, further comprising:

performing linear interpolation on a count in a histogram bin when the count is divided between two CCDF bins.

Claim 17 (Original): The method of claim 12, wherein the plurality of power data values comprise a plurality of $(I^2 + Q^2)$ data values.

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Claim 18 (Original): The method of claim 17, wherein converting the power data value to a floating-point number comprises computing an exponent and a mantissa for a floating-point number according to the equations:

exponent = 2^E–1 – (number of leading zeros in MS, up to 2^E-1)
mantissa = MS[(N-2^E-1+exp):(N-2^E+exp-M)] for exp>0; or
mantissa = MS[(N-2^E):(N-2^E+1-M)] for exp=0

where E is the number of bits assigned to the exponent, M is the number of bits assigned to the mantissa, MS is a respective ($I^2 + Q^2$) data value in the plurality of ($I^2 + Q^2$) data values, and N is the number of bits assigned to the power data value.

Claim 19 (Original): The method of claim 18, wherein the total number of histogram bins in the memory is determined by the equation $2^{(E+M)}$, a maximum bin width is determined by the equation $10^* \log_{10}(1+2^{-M})$, and a range of histogram bins is determined by the equation $(20 - 10^*2^E)^*\log_{10}(2)$.

Claim 20 (Original): The method of claim 12, wherein a maximum count each histogram bin in the memory can accumulate is determined by the equation (2^w-1), where w represents a bit width of the memory.

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